REMARKS

Reconsideration of this application, as amended, is respectfully requested. Claims 1-29 are pending. Claims 1-29 are rejected.

Claims 1, 14, 21, and 27 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Rejections Under 35 U.S.C. § 103

Claims 1-5, 14-18, 21-24, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Value Speculation Scheduling for High Performance Processors" by Fu et al. (art of record, "Fu").

Applicants have amended claim 1 to indicate that the outcome of the second instruction represents a key into a software structure that includes a set of keys representing various outcomes of the second instruction and a corresponding set of predicted outcomes of the first instruction.

The Examiner acknowledges that Fu does not disclose "the outcome of the second instruction represents a key into a software structure that includes a set of keys and a corresponding set of predicted outcomes of the first instruction" (Office Action, pages 3 and 5, 06/24/05).

However, the Examiner states that " Fu does disclose that the set of indexes or keys into the table is assigned to avoid unnecessary conflicts (see, for example, page 264, column 1, lines 29-33) and contends that " it would have been apparent one of ordinary skill in the art at the time the invention was made that the index or key into the table could be designated as the outcome of the second instruction, or any such value, so long as unnecessary conflicts are avoided" (Office Action, pages 3-4, 06/24/05).

Applicants respectfully disagree. Fu discloses predicting the value of the preceding instruction I3 and using LDPRED instruction to load the predicted value into the register R8. The predicted value of the preceding instruction I3 is an operand of the instruction I4 that follows the instruction I3. (p.264, col.1, lines 6-13). The actual result of the predicted instruction I3 is stored in register R4. When predicted value of instruction I3 is incorrect (R8≠ R4), the instruction UDPRED updates the value predictor, which predicts the value of preceding instruction I3, with the actual result of the predicted instruction from register R4 to reset the value predictor (P.264, col. 1, lines 14-28).

Importantly, Fu discloses

> Each LDPRED and UDPRED instruction pair that corresponds to the same value prediction uses the same table entry index into the value predictor.
>
> (Fu, p. 264, col. 1, lines 29-33).

Hence, Fu merely discloses table entry indexes for load instruction LDPRED and update instruction UDPRED that correspond to predicted values of preceding instruction I3 in contrast to table entry indexes that represent various outcomes of the preceding instruction, as recited in amended claim 1. Moreover, table entry indexes in Fu at most correspond to predicted values of preceding instruction I3, and not to a corresponding set of predicted outcomes of the first instruction (I4), as recited in amended claim 1. It is respectfully submitted that if the index into the table of Fu were designated as the outcome of the first instruction (I4), the value predictor of Fu, which predicts the values of the preceding instruction I3, will not operate. Accordingly, Fu fails to disclose, teach, or suggest the limitations of the present invention that are included in the following language of claim 1:

> A method comprising:
> creating a data flow graph associated with a program;
> identifying a first instruction that is to be executed after a second instruction;
> determining that an outcome of the first instruction is dependent on an outcome of the second instruction based on the data flow graph, the outcome of the second

instruction representing a key into a software structure that includes a set of keys representing various outcomes of the second instruction and a corresponding set of predicted outcomes of the first instruction; and

inserting a third instruction to be executed after the second instruction and before the first instruction, wherein the third instruction is to retrieve a predicted outcome of the first instruction from the software structure based on the outcome of the second instruction.

(Amended claim 1) (emphasis added)

Therefore, Applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103 (a) over Fu.

Given that amended independent claims 14, 21, and 27 contain at least the discussed above limitations of amended claim 1, Applicants respectfully submit that claims 14, 21, and 27 are likewise not obvious under 35 U.S.C. § 103 (a) over Fu.

Given that claims 2-5, 15-18, 22-24, and 28 depend from amended independent claims 1, 14, 21, and 27 respectively, and add additional limitations, Applicants respectfully submit that claims 2-5, 15-18, 22-24, and 28 are likewise not obvious under 35 U.S.C. § 103 (a) over Fu.

Claims 6-9, 19, 25 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fu, as applied to claims 1, 14, 21 and 27 above, respectively, in view of U.S. Pat. No. 6,308,322 to Serocki et al. (art of record, "Serocki").

With respect to amended claim 1, as set forth above, Fu fails to disclose the limitations of the outcome of the second instruction representing a key into a software structure that includes a set of keys representing various outcomes of the second instruction and a corresponding set of predicted outcomes of the first instruction.

Serocki discloses predicting indirect branch target addresses using target address hints. The hints comprise most likely indirect branch target addresses (col. 7, lines 30-35).

Thus, Serocki merely discloses determining, for indirect branch target branch prediction, most likely target addresses, in contrast to using an outcome of the second instruction as a key

into a software structure that includes a set of keys representing various outcomes of the second instruction and a corresponding set of predicted outcomes of the first instruction, as recited in amended claim 1.

Thus, neither Fu, nor Serocki discloses, teaches, or suggests such limitations of amended claim 1.

Therefore, Applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103 (a) over Fu, in view of Serocki.

Given that amended independent claims 14, 21, and 27 contain at least the discussed above limitations of amended claim 1, Applicants respectfully submit that claims 14, 21, and 27 are likewise not obvious under 35 U.S.C. § 103 (a) over Fu, in view of Serocki.

Given that claims 6-9, 19, 25 and 29 depend from amended independent claims 1, 14, 21, and 27 respectively, and add additional limitations, Applicants respectfully submit that claims 6-9, 19, 25 and 29 are likewise not obvious under 35 U.S.C. § 103 (a) over Fu, in view of Serocki.

Claims 10-13, 20 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fu, as applied to claims 1,m 14 and 21 above, respectively, in view of U.S. Pat. No. 6,687,807 to Damron (art of record, "Damron").

With respect to amended claim 1, as set forth above, Fu fails to disclose the limitations of the outcome of the second instruction representing a key into a software structure that includes a set of keys representing various outcomes of the second instruction and a corresponding set of predicted outcomes of the first instruction.

Damron discloses an additional memory hardware to store prefetch addresses (col. 4, line 37-col. 5, line 27) in contrast to using the outcome of the second instruction representing a key into a software structure that includes a set of keys representing various outcomes of the second

instruction and a corresponding set of predicted outcomes of the first instruction, as recited in amended claim 1.

Thus, neither Fu, nor Damron discloses, teaches, or suggests such limitations of amended claim 1.

Therefore, Applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103 (a) over Fu, in view of Damron.

Given that amended independent claims 14, 21, and 27 contain at least the discussed above limitations of amended claim 1, Applicants respectfully submit that claims 14, 21, and 27are likewise not obvious under 35 U.S.C. § 103 (a) over Fu, in view of Damron.

Given that claims 10-13, 20, and 26 depend from amended independent claims 1, 14, and 21 respectively, and add additional limitations, Applicants respectfully submit that claims 10-13, 20, and 26 are likewise not obvious under 35 U.S.C. § 103 (a) over Fu, in view of Damron.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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